**IOSR Journal of Engineering (IOSRJEN)** **www.iosrjen.org**
ISSN (e): 2250-3021, ISSN (p): 2278-8719
PP 11-18

# Resource Efficient Multi Ported Sram Based Ternary Content Addressable Memory

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***Abstract:*** *Static Random Access Memory Is Constructed From Ternary Content Addressable Memory Which Provides TCAM Functions By Following It With SRAM. However In SRAM, The Following Of TCAM Suffers From Reduced Memory Efficiency While Map In The TCAM Table. This Is Because Of Low Physical Address And Limited Capacity In SRAM. The Optimal Resource Of Memory Architecture Is Resource Efficient Of TCAM. The Address Information Or Stored In Multiple Virtual Blocks Of SRAM Which Is Presented In The TCAM Table. In Mapping A Greater Position Of TCAM It Increases The Overall Address Space In SRAM Unit. The Overall Followed TCAM Bits/SRAM In A Reduced Throughput. A 512 X 72bit Of Resource Efficient SRAM Based TCAM Consumes A Few Distributed Rams Via Implementation On Xilinx SPARTAN LX9 Field Programmable Gate Array. When Comparing To The Conventional SRAM Based TCAM It Utilizes Only 3.3% Of Memory.*

***Key Words -*** *Field Programmable Gate Array (FPGA), Memory Architecture, Memory Throughput, SRAM Based Ternary Content Addressable Memory, Static Random Access Memory (SRAM).*

## I. Introduction

The main function of Ternary Content Addressable Memory (TCAM) is to explore the contents stored in the SRAM memory. This is searched by accessing of the data by a content not by an address. This is different from a static random access memory because static random access memory which is used to search the content by means of memory. The search query is compared to the TCAM with the contents that are already loaded in entire memory continuously and originated results. In the three states the TCAM can be used as follows two binary states 0's and 1's and don't care states (X). Data cells stores the binary cells and mask cells stores the don't care cells.

The representative TCAM has the primary advantages of quick searching when compared to the SRAM but it also has a limitations. The more transistors are used in TCAM cells so the memory storage has the high production cost per bit and low storage efficiency than SRAM care. This is mainly due to don't care states the additional hardware is needed in terms of bits. To control such limitation in the representative TCAM such as high energy consumption heavy licensing, limited storage capacity, poor scalability and high cost by some TCAM vendors.

The SRAM is required to map TCAM bits in the SRAM based TCAM memory architecture. In the search operation the binary query string of fixed length is required. It creates the vector in the matched address location. The logical one is created as a matched location and zero treated as a mismatched location. When the multiple matched bits are in the vector table the priority encoder is used to prioritize the location.

The data's are stored in SRAM by an sequential manner the following of TCAM as more significance in the usage of decreasing memory efficiency it mainly concentrated in memory and throughput. The following architecture is to make use of memory throughput trade off.

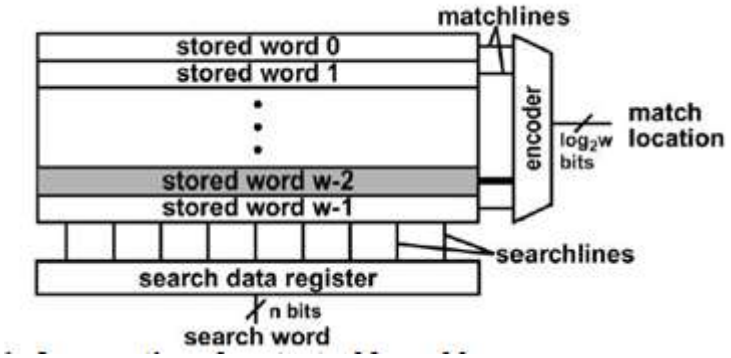


**Fig.1. operation of content addressable memory**

The rest of the brief is as follows. In the section II previous works on SRAM based TCAM. Section III discussed about proposed of low power multi-port resource efficient SRAM based TCAM architecture. Section IV discusses the virtual blocks of memory architecture. The results analysis and comparison of conventional SRAM based TCAM and multi ported resource efficient SRAM based TCAM are discussed in section V. section VI shows the hardware implementation on FPGA section VII concludes this brief.

## II. Prievious Works On Sram Based Tcam

In FPGA flat form several SRAM based TCAM have been

implemented it is implemented on Xilinx FPGA it consists of primitive blocks of RAMS the rams are divided into BRAMs and distributed rams during the search operation the overall power consumption increases and SRAM are activated. To avoid the power consumption low power resource efficient search operation is proposed. The FPGA based classification engine and UETCAM are executed using Altera and Xilinx respectively.

The relatively small TCAMs are divided logically from larger TCAM the researcher HP TCAM hybrid portion and SRAM based TCAM ZTCAN and ETCAM. The SRAM architecture is divided into two. The presence of QS is stored in SRAM the address information of particular QS in stored in second SRAM.

rest memory architecture to achieve a reduced throughput and memory efficient. In the single rest architecture the high level organization of W X H-W Addresses and H bit of inputs clocks and outputs are shown in fig. the construction of rest block consists of consists of virtual blocks, single port architecture, a single multiplexer with an m inputs, and a single de multiplexer with m outputs, priority encoder and w bit blocks of output.

The input of H bit with query strings is divided into large number of B bit substrings. The divided substrings are used as an address in the distributed RAMs with the length of 2b x 1 bit

The distributed RAMs are used as an early elimination table in rest memory architecture. The data that present in the distributed ram are used to find the early elimination of substrings in B bit. The outputs of distributed RAMs are single bit output. The outputs are ANDed to form a single ENABLE signal to the virtual table. When the ENABLE signal is logically low the rest architecture is inactivated.

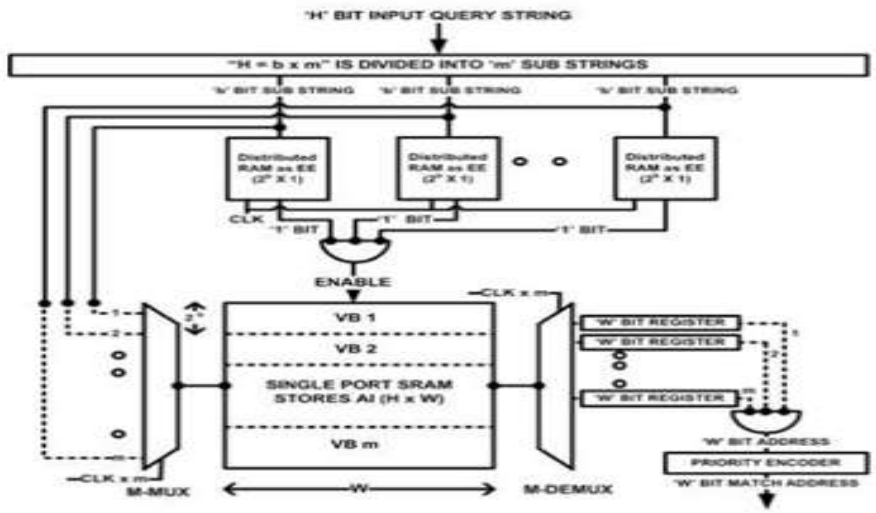


**Fig.2. Memory architecture of a single REST block of dimension**.

In addition to the storage of first SRAM in HP TCAM and the second TCAM is later used for generation of address. In the previous work the consider throughput of resource in a following of TCAM consumes huge SRAM. The explosion of SRAM bits in different physical block is essential to have emulation scheme in architecture. Thus the multi ported resources efficient is proposed.

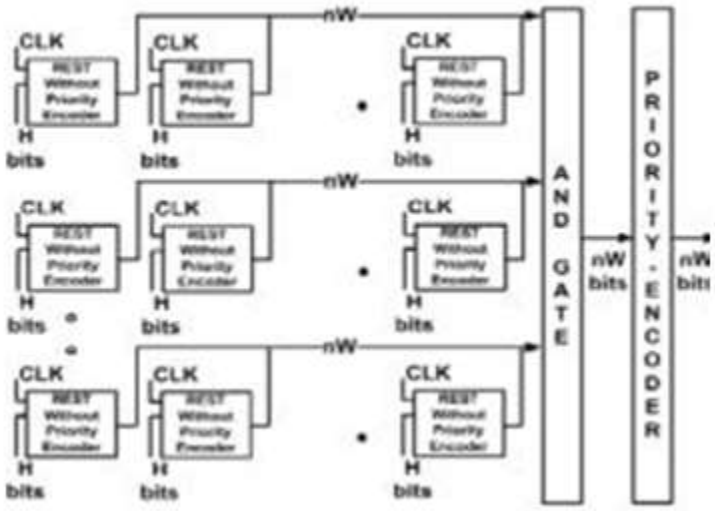


**Fig. 3.** Organization of the REST blocks to create larger TCAM.

## III. Proposed Of Low Power Multiport Sram Based Tcam

The following of rest memory architecture is derived from classical TCAM for resource efficient ways the same size of strings are searched against QS in a TCAM and strings matches the address are terminated as outputs

The virtual blocks in the SRAM plays an important role in

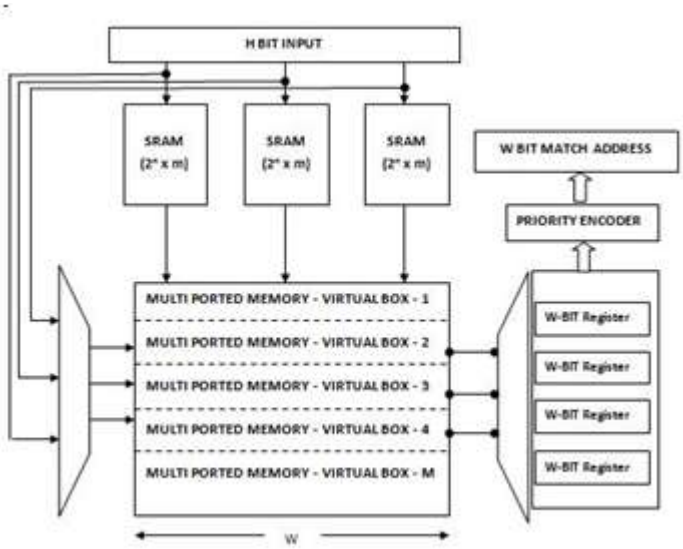


**Fig. 4. Organization of multiport REST blocks to create larger TCAM.**

The B bit substrings are correspondingly given to the M bit multiplexer the clock of M bit inputs are also given to the multiplexer. The virtual blocks are $2^b$ X W bits and the original address of W bit has the same data which B bit substring used. The single post SRAM stores AI which is H X W. The matched address of query string with preloaded data from the single post SRAM with the combination of virtual blocks are directed to M bit de-multiplexer with corresponding W bit register .

## IV. Virtual Blocks Of Memory Architecture

The single port SRAM has the w-bit address and $2^n$ address. The w-bit address and n-bit data stream are used to store in TCAM table for the process of following of TCAM. AI table is corresponding to the w-bit. The original address position of w-bit represents the storage of query string. The type of mapping the relation of SRAM and TCAM are as follows,

SRAM UNIT (2nxw=TCAM (WXN)) (1)

The equation shows that SRAM based TCAM can follows size up to down bit and $2^n$xw. Each size of virtual blocks

2

contains TCAM functionality. The rest memory architecture consists of SRAM with virtual blocks. When the virtual blocks increases Emulated TCAM Bit (ETB) also increases. It consumes large number of bit that available in SRAM. This is known as maximal memory efficiency. AI in the SRAM unit allow only limited TCAM bit to add a more number of

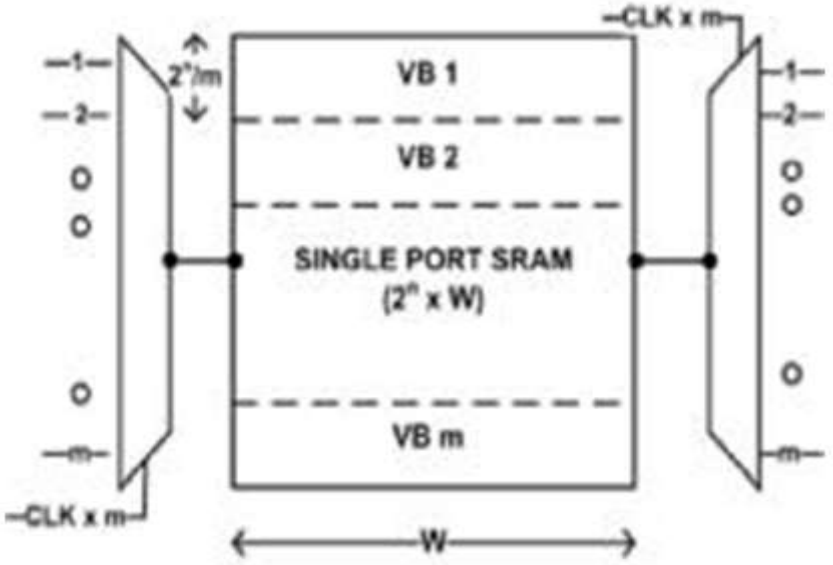


**Fig. 5. VBs of single-port SRAM unit.**

limited memory resources. The SRAM based TCAM does not give the required throughput because of ETB that has limited of SRAM size in the application specific integrated circuits (ASIC).

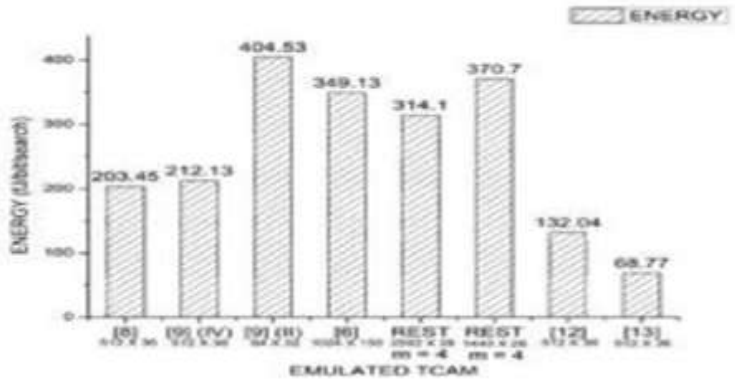


**Fig. 7. Analysis of energy/bit/Search of emulated CAM Architectures**.

A comparison with the conventional TCAM structure the multiport resource efficient SRAM based TCAM has built from m to obtain ETB, latency and throughput. To the best of our knowledge, this is the first work to show relationship between performance parameters of ternary content addressable memory architecture TCAM bit the large number of SRAM required. To overcome the problem the SRAM is half divided address space. The mathematical equation has the pre parameters that are (m, n, W)

ETB=m x {w x (n-log2m)} (2)

**4.1 Throughput ETB tradeoffs:**

The comparison of ETB and throughput were in bits and megabit respectively. The clock frequency of 500MHZ that are operated in 512X72 SRAM 1 to 128 of virtual blocks in SRAM increases to 648 to 18432 bits.

The decreases in throughput from 36 gigabit to 281 megabit. The throughput is a calculation of product of clock and W bits. A throughput can be calculated in single rest block. The address bit per second is produced in a rest block is called throughput. The clock frequency is depended on maximum frequency. The increase in maximum frequency decreases the clock frequency so that the throughput is reduced.

Throughput = clock x W (3)

The virtual block in the rest memory architecture

m is always is greater than 1 when ETB values are calculated without virtual blocks than the m=1. This causes the SRAM based TCAM are implemented in practical design

## V. Result Analysis And Comparison:

### *5.1 Energy Efficiency Analysis:*

When comparing to the various TCAM energy efficiency the proposed multiport REST become efficient. The X-axis shows the sizes and cases of emulated TCAM and Y-axis shows the energy per bit.


**Fig.8**. analysis of number of slice register

### 5.2 Memory Efficiency Analysis:

When compared to single port resource efficient SRAM based TCAM of 72 x 28 with SRAM based TCAM of 512x72 the physical memory is increased

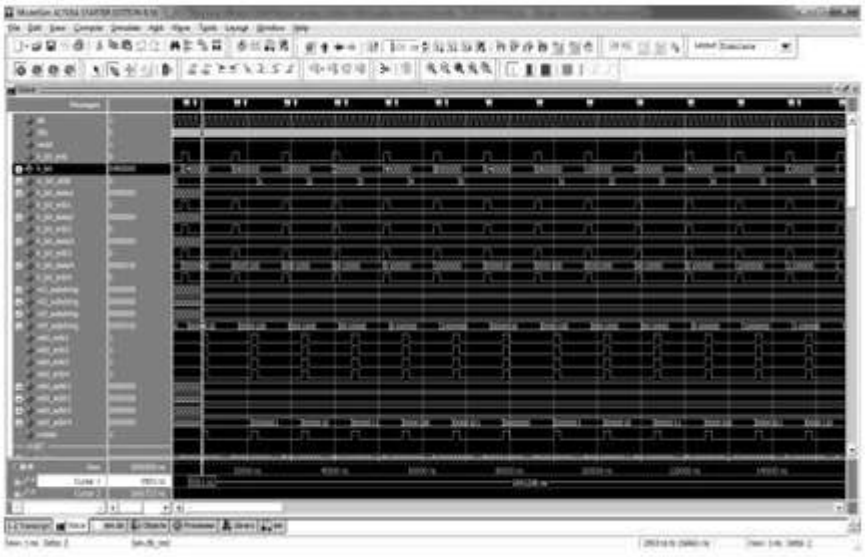

**Fig.9.** output of SRAM based TCAM with 72 x28

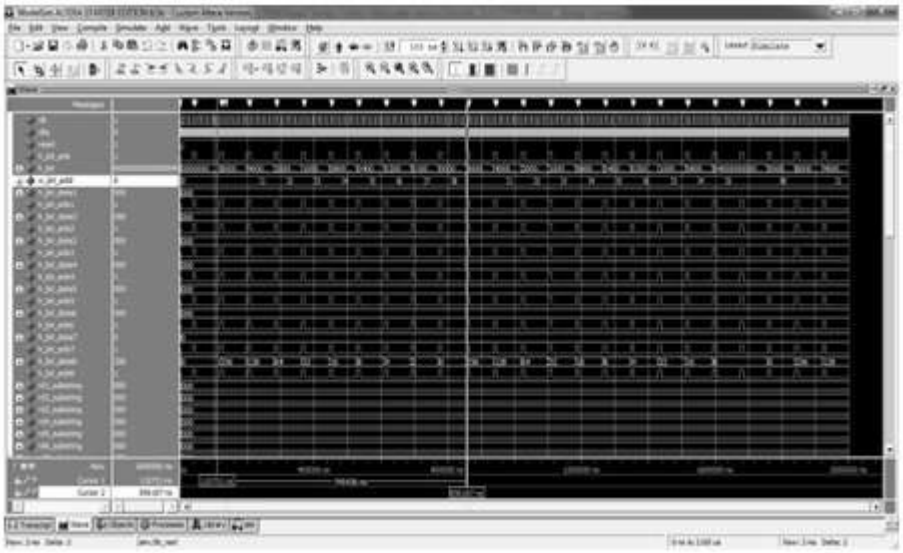

**Fig.10.** output of SRAM based TCAM with 512X7 2

**5.3 Area And Power Analysis:**

The area and power analysis of SRAM based TCAM is computed using the Xilinx x power tool for worst case scenario, in which BRAM and logic blocks are activated and low power is consumed.

The store latency is defined as maximum number of clock cycles which is required to write operation. TCAM array size of 512 x72 requires 513 cycles as a word.

**Fig.11**. power report of 72x28

**Fig.12**.power report of 512 x 72

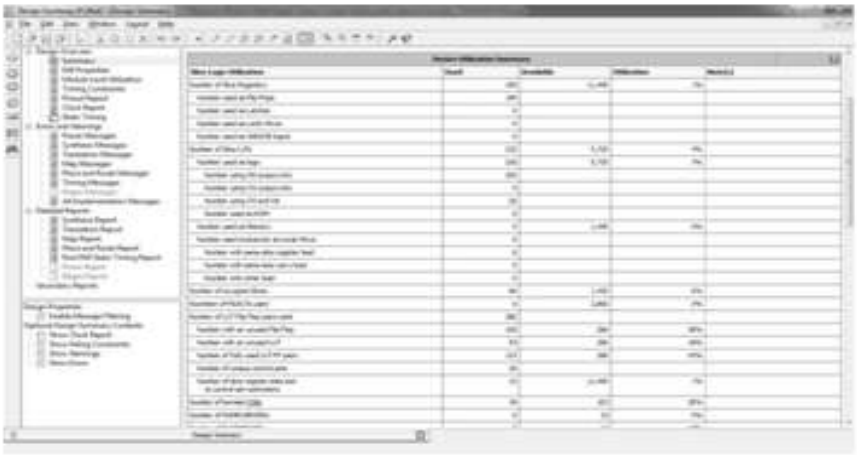

**Fig.13.**area analysis of 72 x28

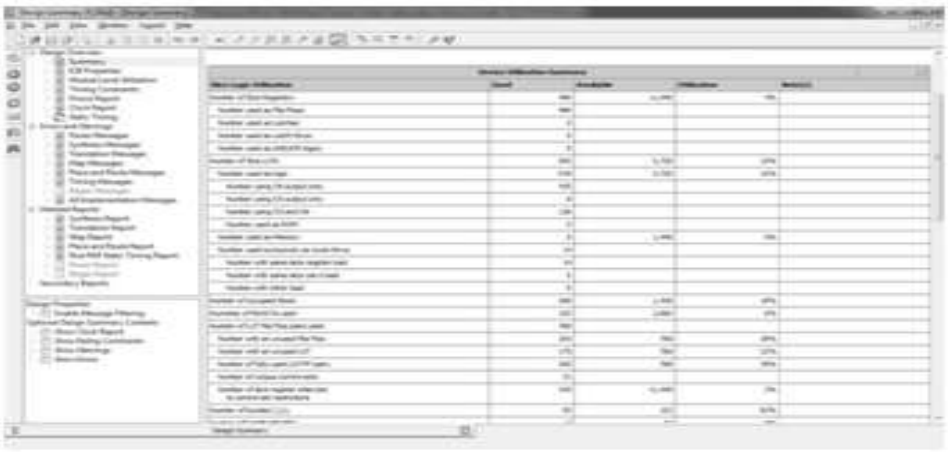

**Fig.14**.area analysis of 512x72

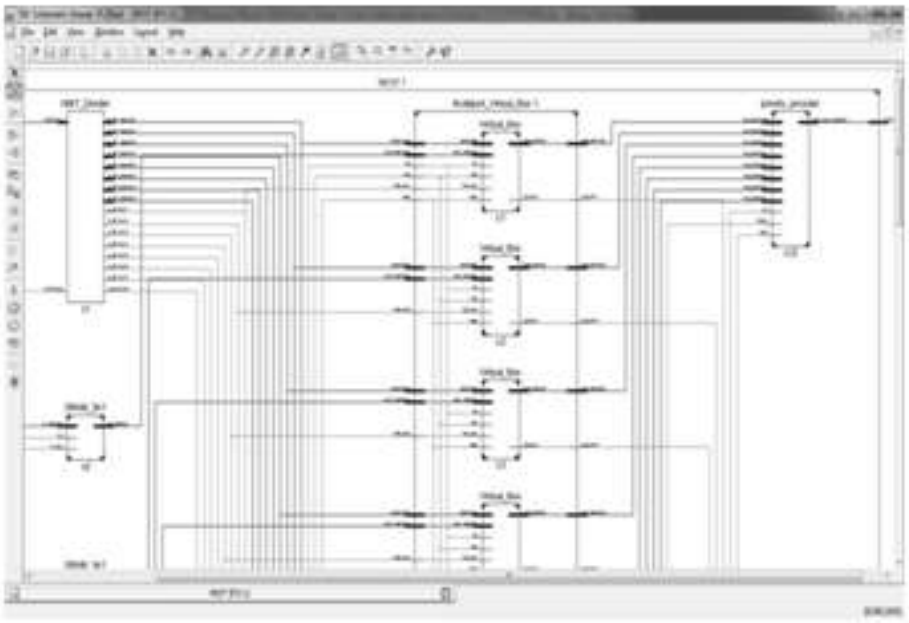

**Fig.15** RTL veiw of multiport REST architecture

## VI. Hardware Implementation:

The existing rest block of 72 x 28 has implemented in Xilinx KINTAX 7 FPGA. The rest block has four virtual blocks system clock of 50MHz.

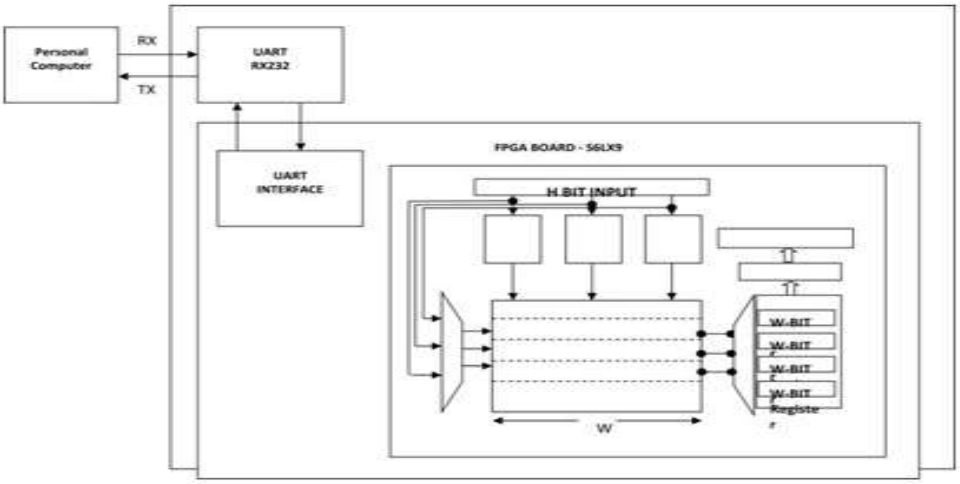


**Fig.16**. Block Diagram Of Hardware Implementation

### 6.1 Power Consumption:

The dynamic power consumption in megahertz in the 72 x 28 rest block for the worst case the power consumption or computed in Xilinx. Logic blocks and BRAMs are activated and there is no power reduction.

### 6.2 Resource Utilization:

In the table 1 shows the resource utilization of 512 x 72 REST block. The column shows their quantity and resources respectively.

## VII. Conclusion

In this brief, we have investigated the trade-off among resources like memory efficiency and throughput in constructing of SRAM based TCAM. The experimental results from the implementation of a multiport 512 X 72 bit REST on FPGA shows a dramatic increase in memory efficiency using four virtual blocks at the cost of reduced throughput. The system uses one 36kb SRAM and eight 64x1 distributed RAM which is equal to 25.3% and 3.5% of memory resources when compared with the ZTCAM and HP TCAM respectively.

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